What is Claimed is:

1. A method of forming contact structures for a semiconductor assembly comprising:

forming a patterned masking material comprising either photoresist or amorphous carbon over contact locations between transistor gate structures;

forming a dielectric material over the patterned masking material and on trench isolation areas underlying a portion of a transistor gate structure lying outside the patterned mask material;

planarizing the dielectric material and the patterned mask material to a level of an insulating cap material covering each transistor gate structure;

removing the remaining planarized patterned mask material to expose the contact locations;

forming a conductive material on the planarized dielectric material, over the transistor gate structures and into the contact locations to make contact to underlying source/drain regions of the transistor gate structures; and

planarizing the conductive material to a level of the planarized dielectric material and to the level of the insulating cap material.

2. The method of claim 1, wherein the forming of the dielectric material comprises a dielectric deposition process utilizing a deposition temperature of approximately 600°C or lower.

3. The method of claim 1, wherein the forming of the dielectric material comprises a dielectric deposition process utilizing a deposition temperature of approximately 550°C or lower.

4. The method of claim 1, wherein the forming of the dielectric material comprises depositing an oxide material utilizing a deposition temperature of approximately 550°C or lower.

5. The method of claim 1, wherein the removing of the remaining planarized patterned comprises dry development processing utilizing an O_2/SO_2 etch chemistry.

6. The method of claim 1, wherein the forming of the conductive material comprises forming a conductively doped polysilicon.

7. A method of forming contact structures for a semiconductor assembly comprising:

forming a patterned masking material over contact locations between transistor gate structures;

forming a dielectric material over the patterned masking material and on trench isolation areas underlying a portion of a transistor gate structure lying outside the patterned mask material, the dielectric material formed by a dielectric deposition process utilizing a deposition temperature of approximately 550°C or lower;

planarizing the dielectric material and the patterned mask material to a level of an insulating cap material covering each transistor gate structure;

removing the remaining planarized patterned mask material by a dry development processing utilizing an O_2/SO_2 etch chemistry to expose the contact locations;

forming a conductively doped polysilicon material on the planarized dielectric material, over the transistor gate structures and into the contact locations to make contact to underlying source/drain regions of the transistor gate structures; and

planarizing the conductively doped polysilicon material to a level of the planarized dielectric material and to the level of the insulating cap material.

8. A method of forming contact structures for a semiconductor assembly comprising:

forming an amorphous carbon over a semiconductor assembly comprising transistor structures having transistor gate structures, source/drain regions set in defined transistor active area regions separated by transistor isolation regions;

forming a patterned masking material over the transistor isolation regions and exposing the amorphous carbon overlying the defined transistor active area;

removing the exposed amorphous carbon to expose contact locations between each transistor gate structure; and

forming a conductive material on the remaining amorphous carbon, over the transistor gate structures and into the contact locations to make contact to the underlying source/drain regions of the transistor gate structures.

planarizing the conductive material and the remaining amorphous carbon to a level of an insulating cap material covering each transistor gate structure;

9. The method of claim 8, further comprising:

removing the remaining amorphous carbon to expose the transistor isolation regions;

forming a dielectric material over the each transistor gate structure and on the transistor isolation regions; and

planarizing the dielectric material to the level of the insulating cap material covering each transistor gate structure.

10. The method of claim 8, further comprising;

forming a protective patterned photoresist over the contact plugs after the removal of the remaining amorphous carbon; and

removing the protective patterned photoresist after the planarizing of the dielectric material.

11. The method of claim 8, wherein the forming of the conductive material comprises a polysilicon deposition process utilizing a deposition temperature of approximately 600°C or lower.

12. The method of claim 8, wherein the forming of the conductive material comprises a polysilicon deposition process utilizing a deposition temperature of approximately 550°C or lower.

13. The method of claim 8, wherein the removing of the remaining amorphous carbon comprises fusion strip/wet clean processing utilizing an O_2 fusion strip, followed by a wet chemistry clean.

14. The method of claim 13 wherein the wet chemistry clean comprises tungsten ammonium hydroxide/hydrogen peroxide mixture (WAPM chemistry.

15. The method of claim 13 wherein the wet chemistry clean comprises ammonium hydroxide/hydrogen peroxide mixture (APM) chemistry.

16. The method of claim 13 wherein the wet chemistry clean comprises hydrofluoric acid (HF) chemistry.

17. A method of forming contact structures for a semiconductor assembly comprising:

forming an amorphous carbon over a semiconductor assembly comprising transistor structures having transistor gate structures, source/drain regions set in defined transistor active area regions separated by transistor isolation regions;

forming a patterned masking material over the transistor isolation regions and exposing the amorphous carbon overlying the defined transistor active area;

removing the exposed amorphous carbon to expose contact locations between each transistor gate structure;

forming a conductively doped polysilicon material on the remaining amorphous carbon, over the transistor gate structures and into the contact locations to make contact to the underlying source/drain regions of the transistor gate structures, the conductively doped polysilicon material formed by a polysilicon deposition process utilizing a deposition temperature of approximately 600°C or lower;

planarizing the conductively doped polysilicon material and the remaining amorphous carbon to a level of an insulating cap material covering each transistor gate structure;

removing the remaining amorphous carbon by a fusion strip/wet clean processing utilizing an O_2 fusion strip, followed by a wet chemistry clean, to expose the transistor isolation regions;

forming a dielectric material over the each transistor gate structure and on the transistor isolation regions; and

planarizing the dielectric material to the level of the insulating cap material covering each transistor gate structure.

18. The method of claim 17, wherein the forming of the conductively doped polysilicon material comprises a polysilicon deposition process utilizing a deposition temperature of approximately 550°C or lower.

19. A method of fabricating a transistor source/drain contact between adjacent transistor gate structures comprising:

depositing a filler material at least in a region between the adjacent transistor gate structures;

removing the filler material with a process having a removal selectivity to nitride greater than 40:1 to form a contact opening; and

depositing a conductive material in the contact opening.

20. A method of fabricating a transistor source/drain contact between adjacent transistor gate structures having nitride sidewall spacers comprising:

depositing a filler material at least in a region between the adjacent transistor gate structures;

removing the filler material with a process having a removal selectivity to nitride greater than 40:1 to form a contact opening having an aspect ratio greater than about 5:1; and

depositing a conductive material in the contact opening.

21. A method of fabricating a transistor source/drain connection between adjacent transistor gate structures comprising:

depositing an amorphous carbon filler material at least in a region between the adjacent transistor gate structures;

selectively dry developing the filler material in the region between the adjacent transistor gate structures to form a contact opening; and

depositing a polysilicon material in the contact opening.